IN THE CLAIMS

Please cancel claims 1-30 without prejudice.

Please add new claims 31-51 as follows:

PENDING CLAIMS ARE AS FOLLOWS

1-30. (Cancelled)

31. (New) A memory control translator comprising:

a first bus interface for a first memory interface, the first bus interface to couple to a memory control unit;

a second bus interface for a second memory interface, the second bus interface to couple to a system memory, the second memory interface differing from the first memory interface;

a command decoder and generator coupled between the first bus interface and the second bus interface, the command decoder and generator to decode and translate commands for the first memory interface from the memory control unit into commands for the second memory interface;

at least one data buffer coupled between the first bus interface and the second bus interface, the at least one data buffer to store data;

at least one address buffer coupled between the first bus interface and the second bus interface, the at least one address buffer to store one or more addresses corresponding to memory locations associated with the data stored in the at least one data buffer;

and wherein the memory control translator to synchronize commands, data and addresses between the memory control unit and the system memory.

32. (New) The memory control translator of claim 31, wherein

the at least one data buffer is a first FIFO buffer.

33. (New) The memory control translator of claim 32, wherein

the at least one address buffer is a second FIFO buffer.

34. (New) The memory control translator of claim 31, wherein

the at least one data buffer includes

a write data buffer for writing data into memory, and

a read data buffer for reading data from memory.

35. (New) The memory control translator of claim 34, wherein

the at least one address buffer includes

a column address buffer to store column addresses, and

a row address buffer to store row addresses.

36. (New) The memory control translator of claim 31, wherein

the first memory interface is an RDRAM memory interface, and

the second memory interface is an SDRAM memory interface.

37. (New) The memory control translator of claim 31 further comprising:

at least one address comparator to compare an address from the memory control unit with an address stored in the at least one address buffer, and

a multiplexor coupled to the at least one address comparator and the at least one data buffer, the multiplexor to select data from the at least one data buffer in response to the at least one address comparator.

38. (New) The memory control translator of claim 37, wherein

the at least one data buffer includes

a write data buffer for writing data into memory, and

a read data buffer for reading data from memory, and

the multiplexor to select data from the write data buffer in response to the at least one address comparator.

39. (New) The memory control translator of claim 38, wherein

the at least one address buffer includes

a column address buffer to store column addresses, and

a row address buffer to store row addresses,

the at least one comparator includes

a column address comparator to compare column addresses, and

a row address comparator to compare row addresses,

and

the multiplexor to select data from the write data buffer in response to the column address comparator and the row address comparator.

40. (New) The memory control translator of claim 36, wherein

the system memory is SDRAM memory and the memory control unit generates commands for RDRAM memory.

41. (New) A memory control translator comprising:

an RDRAM memory interface to couple to a memory control unit;

an SDRAM memory interface to couple to a system memory, the SDRAM memory interface differing from the RDRAM memory interface;

a command decoder and generator coupled between the RDRAM memory interface and the SDRAM memory interface, the command decoder and generator to decode and translate commands received by the RDRAM memory interface from the memory control unit into commands to transmit out over the SDRAM memory interface to the system memory;

at least one data buffer coupled between the RDRAM memory interface and the SDRAM memory interface, the at least one data buffer to store data;

at least one address buffer coupled between the RDRAM memory interface and the SDRAM memory interface, the at least one address buffer to store one or more addresses corresponding to memory locations associated with the data stored in the at least one data buffer;

and wherein the memory control translator to synchronize commands, data and addresses between the memory control unit and the system memory.

42. (New) The memory control translator of claim 41, wherein

the at least one data buffer is a first FIFO buffer.

43. (New) The memory control translator of claim 42, wherein

the at least one address buffer is a second FIFO buffer.

44. (New) The memory control translator of claim 41, wherein

the at least one data buffer includes

a write data buffer for writing data into memory, and

a read data buffer for reading data from memory.

45. (New) The memory control translator of claim 44, wherein

the at least one address buffer includes

a column address buffer to store column addresses, and

a row address buffer to store row addresses.

46. (New) The memory control translator of claim 41, wherein

the system memory is SDRAM memory and the memory control unit generates commands for RDRAM memory, and

the command decoder and generator translates commands for RDRAM memory into commands for the SDRAM memory.

47. (New) A memory control translator comprising:

an RDRAM memory interface to couple to a memory control unit;

an SDRAM memory interface to couple to a system memory, the SDRAM memory interface differing from the RDRAM memory interface;

a command decoder and generator coupled between the RDRAM memory interface and the SDRAM memory interface, the command decoder and generator to decode and translate commands received by the RDRAM memory interface from the memory control unit into commands to transmit out over the SDRAM memory interface to the system memory;

a write data buffer coupled between the RDRAM memory interface and the SDRAM memory interface, the write data buffer to store data to be written into the system memory, and

a read data buffer coupled between the RDRAM memory interface and the SDRAM memory interface, the read data buffer to store data to be read from the system memory;

a column address buffer coupled between the RDRAM memory interface and the SDRAM memory interface, the column address buffer to store one or more column addresses corresponding to memory locations associated with the data stored in the write data buffer and the read data buffer; and

a row address buffer coupled between the RDRAM memory interface and the SDRAM memory interface, the row address buffer to store one or more row addresses corresponding to the memory locations associated with the data stored in the write data buffer and the read data buffer.

48. (New) The memory control translator of claim 47, wherein

the memory control translator to synchronize commands, data and addresses between the memory control unit and the system memory.

49. (New) The memory control translator of claim 47, wherein

the system memory is SDRAM memory and the memory control unit generates commands for RDRAM memory, and

the command decoder and generator translates commands for RDRAM memory into commands for the SDRAM memory.

50. (New) The memory control translator of claim 47, wherein

the write data buffer is a first FIFO buffer, and

the read data buffer is a second FIFO buffer.

51. (New) The memory control translator of claim 50, wherein

the column address buffer is a third FIFO buffer, and

the row address buffer is a fourth FIFO buffer.